Metal oxide nanowire transistors

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Metal oxide nanowires are promising building blocks for thin film transistors due to their one-dimensional geometry in nanoscale, high crystalline nature, and excellent optical and electrical properties. In the past decade, intensive research interest has been drawn to metal oxide nanowire transistors, and various metal oxide nanowires like ZnO, In$_2$O$_3$, and SnO$_2$ have been fabricated into thin film transistors to study their electrical properties and the characteristics as transistor active channels. Much effort has been paid to promote the performance of metal oxide nanowire transistors, and expand the application areas covering from sensing devices, transparent and flexible electronics, to memories and integrated logic circuits. In this review, we highlight the state-of-art progress in metal oxide nanowire transistors, with an emphasis on basic properties and performances. We summarize the characteristics of transistors based on different metal oxide nanowires, the strategies to improve the performance, and various application fields. Finally we present an outlook on the future development of metal oxide nanowire transistors, including the study of material properties, the design of device structures and the development of applications.

1. Introduction

The thin film transistor (TFT) is a special type of field-effect transistor (FET) using thin films of a semiconductor as the active layer, which has been applied for decades, typically in liquid crystal display technology.$^{1-4}$ Owing to some fundamental limit on the material properties and fabrication processes, traditional TFTs based on amorphous or polycrystalline silicon cannot keep pace with the rapid expansion of functional microelectronics, especially the novel transparent and flexible electronics.$^{5-10}$ To meet the demand of these new devices, alternative semiconducting materials are required, with some basic features such as high mobility, compatible fabrication processes with thin film technology, suitable substrates, and excellent transparency or flexibility in some special situations.

Among the various substitutions for silicon based channel materials, low-dimension materials with excellent electrical and optical properties have attracted intensive attention in recent years. Eliminating the limitations of poor material properties, mainly carrier mobility and material stability, suffered by other materials like organic semiconductors and amorphous oxide thin films,$^{11-23}$ these low-dimensional materials present
Potential applications in high performance electronic devices. Great interest has been drawn to single-walled carbon nano-tube (SWNT) and graphene based TFTs due to their fabulous electrical characteristics and excellent performance in high-speed electronics.\textsuperscript{24–30} Radio-frequency transistors have been demonstrated based on SWNTs and graphene with a cutting-off frequency up to 5 GHz\textsuperscript{26} and 100 GHz\textsuperscript{24} respectively. The prominent working speed of these transistors derives from their ultra-high carrier mobilities and saturation velocities, especially the latter has shown carrier mobility exceeding 200 000 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1}\textsuperscript{29} However, it is a big challenge to remove metallic carbon nanotubes from semiconducting ones and control the conducting type and doping level reproducibly.\textsuperscript{27,31–33} While band-gap opening is also an obstacle to graphene.\textsuperscript{34–36}

In contrast, metal oxide nanowires are brilliant semiconducting materials with controllable size and electrical properties, and have attracted great research interests in TFT applications. By vapor or solution method, high quality crystalline semiconducting metal oxide nanowires can be synthesized, with intrinsic superiority in electrical properties over amorphous silicon, amorphous oxide thin films and organic semiconductors, getting rid of the challenges faced by carbon based materials simultaneously. The one-dimensional geometry, sub-micron size, usually large band-gap and excellent properties mentioned above make metal oxide nanowires excellent candidates in high performance TFTs with characteristics of flexibility, high transparency, high carrier mobilities, high on–off ratios, low threshold voltages and steep subthreshold slopes. In addition, metal oxide nanowires are capable to be transferred to all kinds of substrates,

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SN2, Ga2O3, Cu2O and Fe2O3, have been prepared though growth process is catalyzed by the metal decomposed from the process has also been adopted and classified as a branch of VLS bottom-up fabricated electronics. Patterning process, making them perfect building blocks for controllable electrical properties and are suitable for large scale applications. Finally, we conclude this article with a summary of problems remaining and the outlook for future development of metal oxide NW-FETs.

2. Synthesis of metal oxide nanowires

Many kinds of metal oxide nanowires, such as ZnO, In2O3, SnO2, Ga2O3, Cu2O and Fe2O3, have been prepared through numerous routes from simple solution based methods to vapor phase deposition. Among the various methods, chemical vapor deposition (CVD) and hydrothermal/solvothermal techniques are the most popular strategies owing to the simple apparatus utilized.

High quality single crystalline metal oxide nanowires can be synthesized through the CVD method, typically in a horizontal tube furnace. Generally, the source powder is heated at hundreds of or around one thousand degrees Celsius under a flow of carrier gas, and the nanowires are deposited on proper substrates located downstream or upstream to the source powder. The growth of metal oxide nanowires via vapor phase deposition technology is usually described as vapor–liquid–solid (VLS) or vapor–solid (VS) mechanism. In the VLS growth process, metal droplets, usually formed by annealing a gold thin film prepared by sputtering (1–10 nm) or gold colloids, are indispensable to serve as catalysts. These metal droplets capture the source vapor and form liquid alloy droplets, then supersaturation and nucleation happen at the liquid–solid interface, leading to axial crystal growth. Owing to the catalyzed mechanism, the nanowires have diameters equal to the droplets, and only grow at sites activated by metal droplets. ZnO, SnO2, In2O3, Ga2O3 or multicomponent metal oxides, Zn2GeO4, and In2Ge2O7, etc. can be prepared through this method, with controllable diameters and lengths. Fig. 1a and b present ZnO and SnO2 nanowires synthesized by VLS growth method as an example. These nanowires have some common features, such as highly crystalline lattice structure, smooth and uniform cross section, highly anisotropic morphology with large aspect ratio, controllable size and selective space distribution. This unique characteristics imply that VLS grown metal oxide nanowires have excellent and selective space distribution. These unique characteristics determine the growth behavior. Nanowires may have different morphologies like belts, cylinders, needles and so on. For example, Fig. 1c shows a dendritic ZnO nanowire array synthesized using Zn as vapor source.

Much effort has been paid to growing ordered arrays of metal oxide nanowires. In the case of epitaxial growth, substrates play an important role. For instance, vertical aligned tin-doped indium oxide (ITO) nanowire array was synthesized using ITO
thin film as substrate as shown in Fig. 1d.⁵⁴,⁵⁵ Although these highly ordered nanowire arrays are quite tempting for potential applications in large scale patterned functional electronics, they are limited within few kinds of materials for the lack of suitable substrate with tolerable lattice mismatch, which is a problem needing continuous investigations.

For mass production, the solution phase method is a promising route and has been extensively explored to synthesize metal oxide nanowires with the advantages of low cost and easy fabrication and there are various strategies including hydrothermal, solvothermal, sol–gel, refluxing, electrodeposition and so on. Using facile hydrothermal method, our group successfully prepared high aspect ratio ZnO (Fig. 1e) and In₂O₃ (Fig. 1f and g) nanowires with excellent gas sensing performances.⁵⁶,⁵⁷ The ZnO nanowires were obtained by a self-template growth from zinc oleate as precursor, while the In₂O₃ nanowires were achieved after annealing hydrothermally synthesized InOOH nanowires. SnO₂ nanowires can also be prepared via a solution process similar to the synthesis of ZnO nanowires mentioned above.⁵⁸ Other metal oxide nanowires synthesized by hydro/solvothermal method include Cu₂O, Fe₂O₃, VO₂ and so on.⁵⁹–⁶¹ In spite of the decreased crystallinity and weakened electrical properties, it can be predicted that transistors based on these nanowires are very suitable for some specific applications like chemical sensing.

Large aspect ratio is commonly required for nanowires to be used as conducting channel in electronic devices like transistors, which is usually an challenge for general hydro/solvothermal methods however. So various templates have been adopted for solution synthesis of metal oxide nanowires by controlling the material growth in a confined domain or along a specific direction. Among these templates porous membranes are frequently utilized. As a typical example, highly ordered MnO₂ nanowire array with about 40 nm diameters had been direct grown on porous anodic aluminium-oxide/Ti/Si substrate by electrodeposition. During the process, MnO₂ nanowires directly formed in the porous channels of anodic aluminium oxide (AAO) membrane.⁶²,⁶³ Similar method were employed to synthesize Fe₂O₃ and Fe₃O₄ nanowires.⁶⁴,⁶⁵ Besides, carbon nanotubes, surfactants, microemulsions, and surface steps or cracks have also demonstrated to be useful templates for metal oxide nanowires synthesis.

In addition to these broadly applied vapor phase and solution phase methods, some other methods such as electrospinning and simply heating metal foil in air have also been adopted to synthesize different metal oxide nanowires like CuO and Fe₂O₃.⁶⁶,⁶⁷

3. Fundamentals of nanowire transistors

NW-FETs are a kind of FETs, comprising a semiconducting channel made of metal oxide nanowires and a gate to control the conductivity of the nanowire channel by an electric field.⁶⁸ The basic structure is depicted in Fig. 1. The gate is separated from the nanowire by a dielectric layer on back, top or all around the nanowire, named back-gate, top-gate or surrounding-gate FET respectively. The transport characteristics of FETs was analysed by Borkan and Weimer in 1963,⁶⁹ and the gate controlled current can be solved by a successive approximation method. The field effect charge concentration is expressed as

\[ qn(x) = C_g (V_{gs} - V_{th} - V(x)) \]

where \( n(x) \), \( C_g \), \( V_{th} \) and \( V(x) \) refer to carrier concentration, gate capacitance per unit area, threshold voltage and electric potential respectively. The current can be calculated according to the relation \( I(x) = S qn(x) \), where \( S \) refers to the cross section area of the nanowire and \( \mu \) is the carrier mobility. The total current in the nanowire can be calculated as eqn (1) by integrating it along the channel.

\[ I = \frac{1}{2} \mu C_g \left[ (V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \]

by measure the \( I_{ds}-V_{ds} \) and \( I_{ds}-V_{gs} \) curves, we can obtain the electrical properties of nanowires and the transistors. One of the most important figures of merit is the carrier mobility \( \mu \), and it can be determined by transconductance \( g_m \) (eqn (2)) according to eqn (3).

Gate capacitance must be calculated first before analysing the mobility. Unfortunately, it is a complex factor related to the geometry of the nanowire, the structure of the device and the dielectric constant of the insulator. In a typical back-gate NW-FET with a plane gate electrode and a cylindrical nanowire (Fig. 2b), the gate capacitance can be described as eqn (4), which was first carried out by Avouris et al. in their study of carbon nanotube transistors through a numerical calculation method,⁷⁰ and this equation has been widely applied in the NW-FET research field. \( e_r \) is generally defined as the relative constant of the insulator by most of the researchers. However, Lu et al. pointed out that \( e_r \) is actually the average dielectric constant of the device and the medium surrounding the nanowire must also be taken into account.⁷¹ If the nanowire has a belt-like shape (Fig. 2c), the gate capacitor can simply be described as eqn (5) using a parallel plate model, where \( W \) refers to the width of the nanowire.⁷² As to top-gate or surrounding-gate structure (Fig. 2d), the gate capacitance should be calculated as eqn (6).⁷³,⁷⁴

\[ C_G = \frac{2\pi e_r \epsilon_0}{\ln \left( \frac{2h}{r} \right)} L \]

![Fig. 2 Schematics of NW-FET. (a) 3-D view of a back-gate NW-FET. (b) Cross section of cylindrical nanowire back-gate FET. (c) Cross section of belt-like nanowire back-gate FET. (d) Cross section of top-gate NW-FET.](image-url)
Another parameter closely related to the performance and practical application of metal oxide NW-FETs is the threshold voltage $V_{th}$, which is determined by the gate capacitance and the carrier concentration as shown in eqn (7). A relatively higher carrier concentration will lead to a higher threshold voltage and the NW-FET will operate in depletion mode. Increasing the gate capacitance can effectively reduce the threshold voltage.

Other characteristics to describe the performance of a NW-FET include on-off ratio and sub-threshold slope. Among all these factors, mobility and gate capacitance are the most critical ones. Carrier mobility and saturation velocity, which are intrinsic properties of the nanowires, play important roles in the frequency response of NW-FETs. They are closely related to the type of material, impurities, surface defects and so on. Gate capacitance is a controllable factor which can be tuned by the structure of the device and the dielectric constant of the insulator. A larger gate capacitance will lead to a lower threshold voltage, a lower sub-threshold slope and a higher on-off ratio.

### 4. Individual nanowire transistors

#### 4.1 ZnO nanowire transistors

As one of the most prominent materials in the metal oxide family, ZnO has been intensively studied for its versatile physical properties and potential applications in electronics, optoelectronics and piezoelectronics. ZnO is a direct band-gap (3.37 eV at room temperature) semiconductor, with a stable wurtzite crystal structure and polar surfaces. A variety of nanostructured devices, such as ultraviolet lasers, light-emitting diodes, photodetectors and chemical sensors, have been fabricated utilizing ZnO nanowires, due to these unique properties. ZnO nanowires are then configured as FETs.

In typical back-gate configurations at atmosphere environment, the field effect mobility of ZnO NW-FETs falls in the range of 3–40 cm$^2$ V$^{-1}$ s$^{-1}$, with an on-off ratio around 10$^4$ to 10$^7$. It is well known that ZnO nanowires have a large amount of surface defects, mainly oxygen vacancies, that will adsorb gas species and act as scattering and trapping centres. These defects and chemical species have important influences on the performance of ZnO NW-FETs. Hong et al. prepared two kinds of ZnO nanowires on Au-coated substrate and catalyst-free substrate. The catalyzed ZnO nanowires have rougher surfaces and more surface defects, resulting in the depletion mode operation (Fig. 3c and d). Enhancement mode ZnO NW-FET (Fig. 3e and f) are obtained by employing catalyst-free substrate, owing to the reduction of surface defects, which can be confirmed from the decreased PL emission intensity as shown in Fig. 3b. An improved sub-threshold slope can also be observed from the $I_{ds}-V_{gs}$ transfer curve. Realization of highly reproducible ZnO NW-FETs with both depletion mode and enhancement mode has the potential to offer a number of advantages in logic applications.

A novel fabrication method has recently been developed by Kim et al. for ZnO NW-FETs. Patterned multilayer graphene films serves as both growth seeds and source-drain electrodes, upon which the ZnO nanowires can be grown horizontally without metal catalysts with remarkable control of nanowire location. Top-gate structural FETs using these ZnO nanowires present an on-off ratio of 3.98 × 10$^5$, a threshold voltage of −2.27 V and a mobility of ~41.32 cm$^2$ V$^{-1}$ s$^{-1}$.

It is worth noting that high performance ZnO NW-FETs have been demonstrated by Cha et al. with self-aligned planar gate electrodes and well defined nanosize air gap dielectric. These unique ZnO NW-FETs exhibit excellent performance with a transconductance of 3.06 μS, an on-off ratio of 10$^6$ and a field effect mobility of 928 cm$^2$ V$^{-1}$ s$^{-1}$ which is the highest value for ZnO NW-FETs without any specific treatment like passivation.

#### 4.2 In$_2$O$_3$ nanowire transistors

In$_2$O$_3$ is another important metal oxide semiconductor with a wide band gap (a direct band gap of about 3.6 eV and an indirect band gap of about 2.5 eV). Bulk In$_2$O$_3$ thin film has widely been applied in solar cells and light-emitting diodes as

\[
C_G = \frac{\varepsilon_r \varepsilon_0 LW}{h} \quad (5)
\]

\[
C_G = \frac{2\pi \varepsilon_r \varepsilon_0 L}{\ln \left( \frac{R}{r} \right)} \quad (6)
\]

\[
V_{th} = \frac{q\mu}{C_G} SL \quad (7)
\]
transparent electrodes, implying its excellent electrical conducting properties and transparency. Besides, In$_2$O$_3$ nanowires have also been utilized to build high performance FETs. In$_2$O$_3$ nanowires through the VLS method are usually with shorter lengths than ZnO nanowires, but the electronic transport ability is a little bit better. Typically, the carrier mobility ranges about 70–250 cm$^2$ V$^{-1}$ s$^{-1}$. $^{42,84–86}$ However the on–off ratio is about 10$^3$ to 10$^5$, one magnitude lower than ZnO NW-FETs in some cases. As shown in Fig. 4a, $^{46}$ conductance of nanowires increases with the increase of back gate voltage. Using the transconductance obtained from the $I_{ds}$–$V_{gs}$ curve in Fig. 4b, an electron mobility of 98.1 cm$^2$ V$^{-1}$ s$^{-1}$ and 1-dimensional carrier concentration of 2.3 × 10$^{17}$ cm$^{-2}$ were calculated.

It is worth noting that In$_2$O$_3$ nanowires often grow into spiral-like morphology, as a result of the two crystal phases (cubic phase and rhombohedral phase) probably. Our group has investigated these specific nanowires and studied their electronic properties in a back-gate transistors. $^{87}$ Fig. 4c shows the nanowires’ morphology, structure of the transistor and the electronic transport properties. The kinked morphology didn’t affect the performance of the device, and the carrier mobility was estimated to be as high as 243 cm$^2$ V$^{-1}$ s$^{-1}$ from the transfer curve in Fig. 4d, comparable to conventional In$_2$O$_3$ NW-FETs, indicating its promising application in fabricating high performance electronic devices.

### 4.3 SnO$_2$ nanowire transistors

With a wide band gap of 3.6 eV, semiconducting SnO$_2$ has been widely studied and used for transparent conductive electrodes and gas sensing devices. SnO$_2$ has a normal rutile crystal structure and ultralong nanowires and nanobelts of SnO$_2$ can easily be synthesized via the VLS or VS method using SnO$_2$, SnO or Sn as source material, resulting in a big advantage in device fabrication. Wan et al. configured individual SnO$_2$ NW-FETs in a low-cost way, using gold microwire and Ni grid as template to define the source and drain electrodes without using a conventional lithography process (Fig. 5a and b). $^{88,89}$ The linear $I_{ds}$–$V_{th}$ relation in Fig. 5c indicates that this inexpensive method can also ensure good ohmic contact. The current on–off ratio and the sub-threshold slope of the NW-FETs were found to be 10$^4$ and 240 mV per decade respectively, and the carrier mobility was determined to be 12.4 cm$^2$ V$^{-1}$ s$^{-1}$, according to the transconductance calculated from $I_{ds}$–$V_{gs}$ curve in Fig. 5d.

### 4.4 Ternary metal oxide nanowire transistors

While binary metal oxide nanowires have been extensively investigated and fabricated as FET devices, there are still few studies involving ternary oxides, some of which may possess better properties than binary oxides. One of the advantages of ternary oxides over binary oxides is that the properties can be effectively tuned by varying the proportion of each metal component. Studies have verified that bulk Zn$_2$SnO$_4$ crystal has a high thermal stability, high electron mobility, and low visible absorption, making Zn$_2$SnO$_4$ a promising candidates for applications in electronic and optoelectronic devices. $^{90}$ Fig. 6a and b shows the electrical properties of FET based on single Zn$_2$SnO$_4$ nanowire with a smooth cross section. The on–off ratio at 2.0 V bias of $V_{ds}$ (comparing $V_{gs} = -20$ and 20 V) exceeds 10$^4$. And the electron mobility was calculated to be 4.27 cm$^2$ V$^{-1}$ s$^{-1}$. Recently, our group successfully prepared single-crystalline zigzag Zn$_2$SnO$_4$ nanowires as shown in Fig. 6c–e. $^{91}$ Calculated from the measured results, the device shows an on–off ratio of 10$^4$ and a device mobility of 17.2 cm$^2$ V$^{-1}$ s$^{-1}$. Besides, these Zn$_2$SnO$_4$ nanowire-based devices showed a substantial increase in conductance upon exposure to UV light. Thin films of the zigzag Zn$_2$SnO$_4$ nanowires were configured as high performance sensors to detect hosts of chemicals with detection limits down to...
Fig. 6 Electrical transport properties for (a and b) smooth and (c–e) zigzag Zn$_2$SnO$_4$ NW-FET: (a) $I_{ds}-V_{ds}$ curves and (b) $I_{ds}-V_{gs}$ curve of a smooth Zn$_2$SnO$_4$ NW-FET. Reprinted with permission from ref. 90. Copyright: The Royal Society of Chemistry 2011.

Fig. 7 Electrical properties of a lightly Sb-doped SnO$_2$ nanowire configured as a FET device. (a) Family of $I_{ds}-V_{ds}$ curves at different gate-source voltage $V_{gs}$. (b) Transfer ($I_{ds}-V_{gs}$) curve of the same nanowire device at $V_{ds}=0.1$ V. Reprinted with permission from ref. 99. Copyright: 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

the 1 ppm level, especially for ethanol and acetone, showing great potential applications in nanoscale electronics. Although some progress has been made, the field of ternary metal oxide nanowires is still an undiscovered area with sealed properties to be explored.

4.5 Other metal oxide nanowire transistors

In addition to the materials mentioned above, other metal oxide nanowire FETs have also been fabricated to investigate the electrical transport properties. Liao et al. reported individual p-type Cu$_2$O NW-FETs with a high on–off ratio of $10^6$ and high mobility of $>95$ cm$^2$ V$^{-1}$ s$^{-1}$ (ref. 92) CuO NW-FETs were investigated by Li et al. showing a conductivity of $\sim 1.1 \times 10^{-3}$ S cm$^{-1}$, a charge concentration of $9.04 \times 10^{19}$ cm$^{-3}$, and a mobility of $2.51 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ (ref. 92). Fan et al. studied pure Fe$_2$O$_3$ NW-FETs with n-type behavior and Zn-doped Fe$_2$O$_3$ NW-FETs with both n- and p-type conductivity. The charge carrier concentration of Fe$_2$O$_3$ nanowires changed from $5.3 \times 10^{18}$ cm$^{-3}$ to $8.9 \times 10^{19}$ cm$^{-3}$ for n-type doping and $1.2 \times 10^{20}$ cm$^{-3}$ for p-type doping, and the carrier mobilities were estimated to be $2.8 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$, $3.2 \times 10^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$, and $1.3 \times 10^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ for pure, n-type and p-type doped Fe$_2$O$_3$ respectively. Another example is Ga$_2$O$_3$ NW-FET, which has been studied by Chang et al. to show a p-type behavior after Zn-doping with a hole mobility of $3.5 \times 10^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ (ref. 94).

5. Strategies towards high performance nanowire transistors

Although much effort has been given to fabricating FETs with various kinds of metal oxide nanowires and they are proved to be of great superiority over other TFTs made of organic semiconductors and amorphous oxide thin films, the performance of most metal oxide nanowires still cannot compare to conventional top-down fabricated silicon transistors, or compete with FETs based on SWNTs and graphene. We have so far to go before giving full play to the potential of these specific 1-dimensional nanostructures. Recently, to increase the carrier mobility and gate capacitance, which are the most important factors as mentioned in Section 2, different strategies have been studied on the goal of enhance the performance of metal oxide NW-FETs, from modifying the material properties to developing new device structures.

5.1 Doped metal oxide nanowires

Doping is a general route to modify the conducting properties of semiconductors, which changes the carrier concentration, conducting type, band structure, carrier mobility and so on. During the growth process of metal oxide nanowires, it is hardly able to get rid of any unexpected impurities, resulting in unintentional doping and the disparity of the same material prepared by different researchers.

To improve the performance of SnO$_2$ NW-FETs, systematic study of Sb-doped SnO$_2$ nanowires were carried out by Wan et al. Undoped SnO$_2$ nanowire devices show very poor transistor behaviour in air due to their high resistivity and the formation of Schottky contacts. The electrical performance can be significantly improved by Sb doping. Fig. 7a shows the $I_{ds}-V_{ds}$ curves at different $V_{gs}$ from $-4$ V to $+4$ V, for a lightly Sb-doped SnO$_2$ NW-FET. Linear $I_{ds}-V_{ds}$ relation were always observed at low biases, indicating low-resistance ohmic contacts between the nanowire and the Ti–Au electrodes as a result of much higher carrier concentration and disappearance of Schottky barrier. The $I_{ds}-V_{gs}$ curve in Fig. 7b demonstrates that the Sb-doped SnO$_2$ NW-FET operates in n-type depletion mode, with a transconductance of 236 nS and a dramatically increased electron mobility of 550 cm$^2$ V$^{-1}$ s$^{-1}$ at $V_{ds}=0.1$ V. The on–off ratio and sub-threshold slope of the doped device are $10^5$ and 0.17 V per decade respectively. These results confirm that the performance of SnO$_2$ NW-FET can be greatly improved by doping.

Our recent work investigated the As-doped In$_2$O$_3$ NW-FETs, showing a big boost of the electrical performance. The As-doped In$_2$O$_3$ nanowires were configured as transparent thin film transistors (TFTs) with a channel length of 1.8 μm, shown in Fig. 8. The device exhibits typical enhancement mode n-type FET behaviour with a threshold voltage $V_{th}=0.5$ V (Fig. 8b). The doped In$_2$O$_3$ nanowire devices display an on–off ratio...
of 5.7 × 10⁶, and a peak sub-threshold slope of 88 mV per decade. What is amazing is that the device mobility is increased to as high as 1490 cm² V⁻¹ s⁻¹ as the gate bias is increased from 1.0 V to 3.0 V. This value is two orders of magnitude higher than ordinary NW-FETs, indicating that doping is an effective strategy to promote the performance of metal oxide NW-FETs to a level comparable to crystal silicon transistors.

On the other hand, doping is also expected to change the conducting type of metal oxide nanowires, especially p-type doping of ZnO nanowires as an representative, which has been shown to be very difficult and rarely achieved. Group V elements such as phosphorus (P) and nitrogen (N) are generally adopted as dopants for p-type ZnO nanowires and some progresses have been made. Using P₂O₅ or Zn₃P₂ as dopant source, P-doped ZnO p-type nanowires have been demonstrated. However, such p-type conduction is usually unstable and may change to n-type after a period of time in air ambient, probably due to the larger atomic size of P than oxygen. With an atomic radius similar to oxygen, N has been expected to be a better candidate than P for p-type dopant in ZnO nanowires. Using N₂O as a dopant source, Yuan et al. successfully synthesized N-doped ZnO p-type nanowires via a simple reactive CVD process. A transition from n-type conductivity in undoped ZnO nanowires to compensated high-resistive n-type, and finally to p-type conductivity in N-doped nanowires was observed with increasing N₂O in the reaction atmosphere. These p-type ZnO nanowires presented reproducible and stable electrical characteristics with a hole concentration of (1–2) × 10¹⁸ cm⁻³, and mobility of 10–17 cm² V⁻¹ s⁻¹. Although much effort has been paid, reproducible and stable p-type metal oxide nanowires with controllable electrical properties are urgently needed for important applications like complimentary logic circuits.

5.2 Surface passivation

It is well known that surface defect states in metal oxide nanomaterials, typically oxygen vacancies, play an important role in gas sensors. However surface defect states are detrimental factors in NW-FETs by deteriorating the device performance in mobility, on–off ratio and sub-threshold slope. Surface passivation has been adopted to optimize the performance of metal oxide NW-FET. High performance ZnO NW-FETs have been obtained by passivating the surface of nanowires with SiO₂–Si₃N₄ bilayer coating after removing the surface adsorbents such as O₂ and H₂O in a vacuum chamber. The on–off ratio, sub-threshold slope and mobility of untreated FETs are 10³, 3 V per decade and 20–80 cm² V⁻¹ s⁻¹ respectively, while the passivated ZnO NW-FETs exhibit enhanced performances with on–off ratio on the order of 10⁶ and reduced sub-threshold slope of 150 mV per decade (Fig. 9). The mobilities are even increased to 1200–4120 cm² V⁻¹ s⁻¹. Fig. 9a shows the Iₘs–Vₘs curves at different Vₘs, from which clear saturation region and sharp switch of Iₘs can be observed. The origins of the dramatic enhancement come from the passivation of surface defect states which act as scattering and trapping centers, and the reduced chemical species adsorbed at oxygen vacancy sites.

Organic coatings, such as polyimide and PMMA are also utilized to serve as passivation layers for metal oxide NW-FETs. After passivation by these polymer coatings, similar results of enhancement in mobility, on–off ratio, sub-threshold slope and transconductance are also observed. It is worth noting that these metal oxide NW-FETs become more stable regardless of the different oxygen environments after passivation.

Another strategy for passivating metal oxide NW-FETs is annealing in a suitable atmosphere. Myoung et al. compared the electrical properties of HfO₂-gated ZnO NW-FETs after annealed in O₂, N₂ and H₂, and concluded that H₂ annealed ZnO NW-FET had the highest transconductance, on–off ratio and mobility. The enhancement was ascribed to reduced defect site

Fig. 8 Performance of fully transparent As-doped In₂O₃ NW-FETs. (a) Family of Iₘs–Vₘs curves of a single As-doped In₂O₃ nanowire TTFT (b) Current versus gate voltage (Iₘs–Vₘg) plot in the linear regime (Vₘs = 200 mV). (c) Frequency response of AC gain of As-doped In₂O₃ nanowire TTFT. (d) Schematic diagram of As-doped In₂O₃ nanowire TTFT fabricated on an ITO glass substrate. Reprinted with permission from ref. 100. Copyright: 2009 American Chemical Society.

Fig. 9 (a) Iₘs–Vₘs curves of a ZnO NW-FET without surface treatments showing typical n-type semiconducting behaviour. (b) Schematic of ZnO NW-FET passivated by Si₃N₄–SiO₂ bilayer dielectric. (c) Iₘs–Vₘs curves of surface passivated ZnO NW-FET. (d) Semilog plot of Iₘs–Vₘg. Reprinted with permission from ref. 106. Copyright 2006 American Institute of Physics.
density and adsorbed oxygen species between the ZnO nanowire channel and the surface of HfO₂ gate dielectric layer.

5.3 Top-gate and surrounding-gate structures

In addition to modify the materials by doping or passivation, another route to high performance NW-FETs is optimizing the device structure, taking the advantages of the geometry of nanowires, to improve the gating effect by increase the gate capacitance. The various modeling and simulation studies have demonstrated the high device performance of surrounding-gate FETs (SG-FETs), which was first realized by Lieber’s group with Si-Ge nanowires. ZnO nanowire based SG-FETs were subsequently achieved by the NASA group.³ Fig. 10 shows the structure of SG-FET with ZnO nanowire. The ZnO nanowires were vertically grown on SiC substrate, which was directly employed as the source electrode. The gate oxide and gate electrode were fabricated by conformal CVD and conformal ion-beam deposition respectively. After removing excess SiO₂ by chemical mechanical polishing, the drain electrode was formed after partly etching the gate electrode. The fabrication process for vertical SG-FET is so complicated that other researchers built omega-shaped-gate FETs (OSG-FETs) with ZnO nanowires, according to the suggestions that OSG-FETs should exhibit similar device performances to SG-FETs.¹¹⁰,¹¹¹ Fig. 11 shows the cross section of the OSG-FET based on ZnO nanowires, in which the ZnO nanowire is surrounded by the Al₂O₃ gate oxide and Ti–Au gate electrode.²⁴ Compared with conventional back-gate FET, the peak transconductance is increased from 12.5 to 400 nS, the field effect mobility from 8.6 to 30.2 cm² V⁻¹ s⁻¹, and the on–off ratio from 1.09 to 10⁶, indicating remarkable enhancement of electrical characteristics. The enhancement originates from not only the increased gate capacitance induced by OSG geometry, but also the passivation of the ZnO nanowire surface induced by the cladding of Al₂O₃.

Yi et al. built a dual-gate ZnO nanorod FET to compare the top gate and back gate in the same device.¹¹² The top-gate mode shows better electrical characteristics with increased on–off ratio from 10⁴–10⁶ to 10⁵–10⁷ and transconductance from 34 to 240 nS. According to the numerical simulation of the gate electric field in their work, such an improvement is caused by geometrical enhancement of the gate capacitance.

5.4 Optimized insulators

As analyzed in Section 2, gate capacitance is not only related to the geometry and structure of FETs, but also the dielectric layer. It can be improved by either increasing the dielectric constant or reducing the thickness of the insulator. However, using an ultrathin conventional insulator like SiO₂ to increase the gate capacitance is not a good idea, as it will lead to terrible leakage current. So high-κ dielectrics like Al₂O₃,¹¹³ and HfO₂ (ref. 114) are employed to achieve an enhanced gate capacitance by reducing the effective thickness. Besides, some novel dielectrics have been explored and exhibit even better performance than ordinary dielectrics.

Recently high performance NW-FETs using a self-assembled nanodielectric (SAND) as the gate insulator have been demonstrated with ultralow threshold voltage, reduced sub-threshold slope, improved on–off ratio and mobility.¹¹⁵–¹¹⁸ Fig. 12a–d show a back-gate ZnO NW-FET using SAND as ultrathin insulator.¹¹⁶ The SAND dielectric material is composed of self-assembled multilayers that include (Fig. 12b) α,ω-difunctionalized
5.5 Metal contact engineering

The Schottky barrier formed at the source and drain metal–semiconductor interface is another problem affecting the performance of NW-FETs. The height of the barrier is determined by the Fermi level deviation between the metal and semiconductor, so proper metals should be chosen in order to match the Fermi level and lower the barrier. However, optimized combination of the semiconducting nanowire and the metal contact cannot always be reached. Other strategies should be considered such as doping. Carrier concentration will be increased by doping leading to the decrease of barrier width and an improved probability for carriers tunnelling through the barrier. Studies by Wan et al. on doping dependent electrical properties of SnO$_2$ nanowires demonstrated the disappearance of Schottky barrier when Sb was doped into SnO$_2$. To avoid doping induced scattering of carriers, a localized doping may be preferred rather than doping the whole active channel of NW-FET.

To avoid Schottky barrier at the source and drain contact, Lee et al. demonstrated the shift of threshold voltage by employing metals with different work function as the gate electrode, showing that metal contact engineering is a promising method to tune the transfer characteristics of NW-FET which can be used in integrated logic circuits. Using heavily doped p-type SiC as the source electrode, researchers at NASA developed p-channel NW-FET with n-type ZnO nanowire. These examples show that rather than an obstacle, the contact barrier can be employed as an effective tool to control the characteristics of metal oxide NW-FETs through careful design.

6. Applications of nanowire transistors

6.1 Transparent and flexible electronics

One of the most promising applications of metal oxide NW-FETs is transparent and flexible electronics. Optically transparent and mechanically flexible electronic circuits are essential components for the next-generation display technologies, including ‘see through’ and conformal products. Traditional TFTs based on polycrystalline silicon or amorphous silicon which are widely applied in present commercial displays, suffer from the lack of transparency, the main factor limiting the aperture ratio and resolution of the displays. Large bandgap metal oxide nanowires like ZnO, In$_2$O$_3$ and SnO$_2$ are all intrinsically transparent materials, with inherent mechanical flexibility and high carrier mobilities compared with bulk or thin-film materials. So metal oxide nanowires have attracted particular interest for transparent and flexible electronics.

The transparent NW-FETs mainly comprise transparent metal oxide nanowires, transparent conducting electrodes and insulators, as shown in Fig. 13a. Using a SiO$_2$ buffer layer, a patterned IZO gate electrode, an atomic layer deposition (ALD)-derived high-$k$ Al$_2$O$_3$ gate insulator, and single-crystal semiconducting In$_2$O$_3$ and ZnO nanowires as active channel, Ju et al. built TFTs on glass. From the optical transmission spectra and the real device in Fig. 13d, these transparent transistors are of perfect optical transparency with above 90% incident light in visible band passes through the device. Proper transparent electrodes should be selected to lower the contact...
barrier. ITO and IZO are adopted because their basic crystal structures are sufficiently similar to those of In$_2$O$_3$ and ZnO. After ozone treatment, these TTFTs exhibit transfer and current versus voltage ($I_{ds}$–$V_{gs}$) characteristics (Fig. 13b and c) comparable to those observed in non-transparent devices using the same types of materials. Replace the glass substrate with PET, they also fabricated transparent as well as flexible transistors using In$_2$O$_3$ nanowires, with excellent transfer characteristics as shown in Fig. 13e. Other metal oxide nanowires are also utilized as channel materials of TTFTs. For instance, Wan et al. fabricated TTFTs using SnO$_2$ nanowire array assembled by contact-printing techniques. Recentl...
More complicated fully transparent AMOLED displays driving by metal oxide nanowire TFTs were also designed by Ju et al. A 30 × 10 pixel array was built into a 2 × 2 mm display (Fig. 15d and f). The structure of each pixel is presented in Fig. 15g and h, consisting of one switching transistor (T1), two driving transistors (T2 and T3) and one storage capacitor. All the transistors were built using In$_2$O$_3$ nanowires as active channel. Fig. 15e shows the switch of pixel array between on and off state. The optical transmittance of before and after the deposition of OLED with a ultrathin Al cathode were 72% and 35% respectively. And the luminescence of the OLED was 1630 cd m$^{-2}$ within the active pixel area, corresponding to an average luminance of 300 cd m$^{-2}$ for the overall array.

6.2 Gas sensing devices

Sensing behaviour is another of the important and well-known properties of metal oxide nanowires. Due to the one-dimensional geometry that is relatively easy for electrical contact formation, large surface to volume ratios, comparable diameters to Debye length and the widely studied dangling bonds and defects at the metal oxide surface that can attract oxygen from the ambient, metal oxide NW-FETs are promising candidates for high performance gas sensors compared with other systems. A variety of metal oxide NW-FETs have been investigated to detect different gases. The most popular material and gases are ZnO for O$_2$, NH$_3$, NO$_2$, In$_2$O$_3$ for O$_2$, H$_2$, CO, NH$_3$, NO$_2$, and SnO$_2$ for O$_2$, CO. The gas sensing properties rely on the redox reaction between the metal oxide nanowires and the surrounding gases. Briefly, the dangling bonds and surface deficiencies contribute to the adsorption of chemical species. For n-type metal oxides, reducing gases react with the adsorbed oxygen species and release electron into metal oxides, leading to the increase of conductivity, while oxidation gases take an inverse process and trap electron from metal oxides, reducing the conductivity. P-type metal oxides have opposite principles due to the different conducting carriers.

Fig. 16 shows the ZnO NW-FETs for TNT detection as an example. From the $I_{ds}$-$V_{ds}$ curves in Fig. 16b, a decrease of current can be observed as the concentration of TNT increasing from 60 ppb to 1.36 ppm. The time-resolved dynamic response of conductance in Fig. 16c presents seven cycles corresponding to seven different TNT/air concentrations ranging. As depicted in Fig. 16d, the sensitivity follows the equation of $S = \Delta G/G_0 = A/(1 + BC/A)$, where $A = 0.086$, $B = 16.74$ and $C$ refers to the concentration. At lower concentrations, the chemical sensor exhibited a linear dependence between the normalized sensor response and the TNT concentration, while the surface coverage tends to saturate and hence leads to the saturation response observed in Fig. 16d. This is a common phenomenon in metal oxide NW-FET gas sensors. The mechanism of gas sensing properties to TNT is related to the decomposition process of TNT molecules, in which NO and NO$_2$ are the signature decomposition products. NO can react with oxygen species adsorbed on the ZnO nanowire surface, and convert to NO$_2$. The adsorbed NO$_2$ can strongly withdraw electrons and cause a reduced conductance for ZnO NW-FETs.

The conductivity of NW-FETs can be effectively tuned by the gate potential, so it is reasonable to assume that the gate potential has a non-negligible effect on the gas sensing characteristics of metal oxide NW-FETs, which has been seldom reported however. Recently, Mubeen et al. studied the gate-tunable surface processes on Pd-nanoparticle decorated SnO$_2$ NW-FETs with 50 nm thick Al$_2$O$_3$ as gate insulator (Fig. 17), when exposing to H$_2$. As shown in Fig. 17b, the concentration of H$_2$ has a great influence on the electrical transfer characteristics. As the concentration increases, the field effect of gate potential on the current is weakened, and the threshold voltage

![Image](https://example.com/image1.png)

**Fig. 16** (a) Schematic view of a ZnO NW-FET structure. (b) $I_{ds}$-$V_{ds}$ curves taken in air and at different TNT concentrations. (c) Sensing response of a ZnO nanowire chemical sensor to TNT. (d) Normalized conductance change ($\Delta G/G_0$) vs. TNT concentrations ($C_t$), which was fitted using $S = 1/(A + BC)$. Reprinted with permission from ref. 129. Copyright: 2010 WILEY-VCH.

![Image](https://example.com/image2.png)

**Fig. 17** (a) Schematic of the metal-nanoparticle decorated single SnO$_2$ NW-FET gas sensor and its operation. (b) Effect of hydrogen partial pressure on the measured transfer characteristics of Pd-nanoparticle decorated SnO$_2$ nanowire. (b) Measured threshold voltage (red dots) as a function of the square root of the hydrogen partial pressure. (c) Real time conductance ($G(t)$) response of Pd-nanoparticle decorated SnO$_2$ NW-FET plotted as a function of back gate voltage towards 2500 ppm hydrogen. Reprinted with permission from ref. 130. Copyright: 2011 WILEY-VCH.
of the FET increases. The concentration dependent threshold voltage is depicted in Fig. 17c, in which the threshold voltage increases linearly with the square root of the hydrogen partial pressure. The increase of threshold voltage originates from the increase of carrier concentration caused by the reducing gas which release electrons to SnO₂ nanowires. On the other hand, the gate potential has a counter force on the gas sensing properties. As shown in Fig. 17b, the change of current with and without H₂ was effectively tuned by the gate voltage. When the gate voltage is about −3 V, which is in the depletion region, the most significant change can be observed. Fig. 17d demonstrates the time-resolved dynamic gas sensing responses of the device at different gate potentials from −3 V to 2 V, from which the effect of gate potential on sensitivity can be apparently observed. With an optimized gate potential of −3 V, 2500 ppm of H₂ induced an almost 10 000-fold change in the source–drain current, as compared to factors ~60 at zero gate bias.

### 6.3 Photodetectors

Metal oxide NW-FETs are also applied in the area of photodetectors. The basic mechanism of photodetectors is based on the change of carrier concentration induced by light illumination. Because gate potential has a similar function on carrier concentration, the effect of gate potential and the light illumination may interact with each other and present an interesting phenomenon. Kim et al. studied the influence of gate voltage on the response of ZnO NW-FETs under UV irradiation, and optimized the performance as UV photodetectors.⁵⁵ By comparing the electrical transfer characteristics in dark and under UV irradiation, they found that the ZnO nanowire photodetector is most sensitive and has a much faster recovery speed when \( V_{gs} \) is positioned at the “bottom” of the sub-threshold swing region (Fig. 18a). The enhanced sensitivity can be ascribed to the fact that the dark current at the off-state is much smaller than that at the on-state by a factor equal to the on–off ratio of the transistor, while the current under irradiation is almost the same between on-state and off-state. In fact, the sensitivity when the transistor is switched off is just a little bit higher than the on–off ratio of the transistor. So a larger on–off ratio, which can be obtained by tuning the drain bias, leads to an increase of the sensitivity as well, as shown in Fig. 18b. The response speed can also be optimized by control the gate voltage which can be observed in Fig. 18c. When the gate voltage is positioned in depletion region, it can help depleting the photo-induced carriers and accelerate the recovery of the photodetector.

The UV irradiation, in turn, can alter the electrical transfer properties. As shown in Fig. 18d, the irradiation leads to an increase of threshold voltage owing to the raising of carrier concentration. Similar phenomenon has also been observed by Fan et al. in their study of ZnO NW-FETs.⁷⁹ By the way, polarization dependent response of UV illumination was discovered by Fan simultaneously, indicating that nanowires are more sensitive to the light with a parallel polarization to the axis.

It can be extracted from these studies as a common rule, that high sensitive photodetector will have a lower carrier concentration. This is consistent with the study of Wan et al. on doping dependent properties of SnO₂ nanowires, in which the undoped SnO₂ NW-FETs present better performances as photodetectors.⁸⁹

![Fig. 18](image-url) (a) \( I_{ds} – V_{gs} \) characteristics under UV illumination and in darkness when \( V_{ds} = 1 \) V. (b) Linear relationship between photocurrent–dark current ratio \( (I_{ph}/I_{dark}) \) and initial on–off ratio \( (I_{on}/I_{off}) \) of the ZnO NW-FET. (c) Current measured as a function of time \( (I_{ds} – t) \) while the light was on and off at gate voltages of 5 V, 0 V and −5 V. (d) Change of \( I_{ds} – V_{gs} \) characteristics over time after UV light is turned off \( (V_{ds} = 1 \) V). Reprinted with permission from ref. 131. Copyright: 2009 WILEY-VCH.

Metal oxide nanowires are mostly wide band gap semiconductors and visible light cannot generate electron–hole pairs. However, there is another factor affecting the carrier concentration of the metal oxide nanowires. The chemical species adsorbed on the surface of metal oxide nanowires, typically oxygen, can trap electrons and decrease the carrier concentration. On the other hand, it is a well-established fact that the activation energy \( (E_a) \) for oxygen desorption from the ZnO surface is about 1.0–1.1 eV. So a photon-assisted molecule desorption (PAMD) mechanism may lead to sub-band gap photon response, and make metal oxide nanowires sensitive to visible light, by modulating the concentration of surface chemical species and the carrier concentration in succession, as shown in Fig. 19. Liu et al. have practically observed this exciting phenomenon in ZnO NW-FETs.¹² Under the irradiation of white light as well as 633 nm He–Ne laser, the shift of threshold voltage and the change in electrical transfer characteristics can be observed in Fig. 19a and b respectively. The deviation of time-resolved dynamic response under in vacuum and in air indicates that the response is related to the adsorbed oxygen species. The mechanism is presented in Fig. 19d, the interaction of visible light and the surface chemical species results in the change of band structure, the carrier concentration and eventually the ability of detecting visible light.

### 6.4 Biosensors

Biosensors based on nanowire/carbon nanotube transistors are one of the most attractive applications, combining bionanotechnology and microelectronics, in less than a decade. Owing to the absence of native oxide layer which may decrease the
sensitivity, metal oxide nanowires, such as In$_2$O$_3$, ZnO, and SnO$_2$, can easily derivatize and are potential alternative materials to silicon nanowires for biosensing applications. Zhou et al. recently reported their In$_2$O$_3$ NW-FETs with the ability to detect SARS virus N-protein using antibody mimics as capture probes. As shown in the inset of Fig. 20a, the In$_2$O$_3$ NW-FET based biosensors have been configured with AMP (Fibronectin, Fn) as a biomarker, and BSA as passivation to get rid of nonspecific binding interactions of proteins with the nanowire device and probably false positive results. Fig. 20b and c depict the change of normalized current when adding BSA. After several times of BSA addition, the current stabilize as a baseline and are suitable for the detection of N protein. The current responses to different concentration of N protein is demonstrated in Fig. 20d. A higher concentration leads to a larger normalized current response as shown in Fig. 20e. When Fn is removed, no significant response can be observed, confirming that the Fn-based capture probe can selectively capture the N protein.

In another work by Zhou et al., they found that electrostatic interaction is the dominant sensing mechanism for In$_2$O$_3$ NW-FET based biosensors, and studied the correlation between the absolute responses and the gate dependence of biosensors measured by means of liquid gate. They developed a data analysis method to calibrate the sensor performance by dividing the absolute response by the gate dependence of each device and successfully reduced the device-to-device variation according to the correlation.

6.5 Memories, logic gates and circuits

In microelectronics, memories and logic circuit units are the most important components for computing. With excellent carrier mobility, metal oxide NW-FETs are of great potential in applications for high-speed devices and are promising building blocks for novel nanocomputing systems. Towards this goal, some strategies for memories and logic circuits have been designed recently, demonstrating feasibility of utilizing metal oxide NW-FETs as basic element for computing.

One of the widely applied memory configuration is floating-gate structure, which was first considered to build memories based on metal oxide NW-FETs. Yeom et al. embedded Pt nanocrystals in Al$_2$O$_3$ gate oxides and designed ZnO nanowire-based nano-floating gate memory (NFGM). The Pt nanocrystals act as charge storage nodes and lead to the shift of threshold voltage by 3.8 V between on and off state, with a retention time of $5 \times 10^4$ s.

Ferroelectric insulators are also considered to build memories. Liao et al. designed a planer structure employing ferroelectric Pb(Zr$_{0.5}$Ti$_{0.5}$)$_2$O$_3$ (PZT) film as the gate dielectric and the charge storage medium as shown in Fig. 21a–c. The Pt film serves as gate electrode and ZnO nanowires sit horizontally on top of the PZT layer. Fig. 21b and c shows the electric transport properties the ZnO memory. An obvious hysteresis loop with a shift of ~6 V in threshold voltage can be observed. The memory function mainly originates from the nature of PZT ferroelectric, however the effects due to surface molecular adsorption should also be...
counted in. The single ZnO nanowire device exhibits an on–off ratio up to $10^3$.

Nanowire memories based on nanostructured ferroelectric materials are also designed which present better performances than ferroelectric film based memories.\textsuperscript{139} As shown in Fig. 21d–f, this kind of memories is a combination of a stable ZnO nanowire as a semiconducting channel, which is beneficial for tuning and controlling channel conductance due to the large surface to volume ratio, and inorganic ferroelectric nanoparticles as the gate dielectric surrounding the channel surface. The electrical characteristics in Fig. 21e demonstrate that with back-gate configuration, the threshold voltage can be shifted as large as 11 V. The different circulation direction between back-gate (Fig. 21e) and top-gate (Fig. 21f) configurations confirms that the hysteresis behaviours originate from the effect of ferroelectric nanoparticles. Owing to the advantages of nanostructured ferroelectric particles, the device possesses an on–off ratio exceeding $10^4$, and a long retention time of over $4 \times 10^4$ s.

To demonstrate the potential of metal oxide NW-FETs as multifunctional devices, integrated logic circuits fully based on n-type ZnO nanowires have been carefully designed and developed.\textsuperscript{140–143} For instance, Park et al. built Schottky diodes and metal semiconductor field effect transistors (MEFETs) employing Au as Schottky contact and Schottky gate electrode respectively.\textsuperscript{144} Combing the Schottky diodes and MEFETs, logic gates with function of OR, AND, NOT and NOR are developed. Similar devices have been fabricated by Kaelblein et al. using ZnO NW-FETs with self-assembled monolayer gate dielectric.\textsuperscript{117}

To lower the power consumption, a complimentary configuration combining n-type and p-type semiconductors is preferred. However, most metal oxide nanowires like ZnO, In$_2$O$_3$ and SnO$_2$ are n-type semiconductor, so they should be integrated with other materials. N-type ZnO nanowires have been demonstrated to incorporate with p-type SWNTs and built into logic gates with different functions.\textsuperscript{145} In complimentary circuits, the threshold voltage must matched well, which is achieved by proton irradiation. The threshold voltage of ZnO NW-FET is sensitivity to proton irradiation, which is out of operation for SWNT transistors. So the threshold voltages can be matched as shown in Fig. 22b. After proton irradiation, an improved gain can be obtained in an inverter which outputs perfect response to input signal (Fig. 22c). Through properly assembling n-type ZnO NW-FETs and p-type SWNT transistors, NOR gate, NAND gate and flip-flop SRAM are demonstrated as well (Fig. 22e).

It is worth noting that for practical large scale fabrication of metal oxide NW-FETs and some applications, a low-cost and efficient method to assemble and integrate nanowires in an ordered manor must be developed. It has been summarized in another review article specially,\textsuperscript{146} but it is not the key point to be discussed in this article.

Fig. 21 (a–c) ZnO NW-FET memory using planar PZT ferroelectric as gate oxide: (a) schematic of the memory device structure; (b) $I_{ds}$–$V_{ds}$ output characteristics and (c) $I_{ds}$–$V_{gs}$ transfer characteristics at $V_{ds} = 2$ V. Reprinted with permission from ref. 138. Copyright: 2009 American Chemical Society. (d and e) ZnO NW-FET memory utilizing ferroelectric nanoparticles: (d) schematic of the device structure; (e) a hysteretic behaviour for a back-gate ZnO NW-FET after coating FENPs on the NW surface; (f) hysteresis behaviours of a top-gate NW-FET as a function of the sweep range of gate voltages. Reprinted with permission from ref. 139. Copyright: 2010 American Chemical Society.

Fig. 22 (a) Schematic of the hybrid complementary logic circuit comprising n-channel ZnO nanowire and p-channel SWNT-network FET devices irradiated with proton beams. (b) An overlay of $I_{ds}$–$V_{gs}$ curves ($V_{ds} = 1$ V) of the ZnO-nanowire and SWNT-network FETs before and after proton irradiation. (c) VTCs of a complementary inverter with changes in the switching voltage and inverter gain before and after proton irradiation. (d) Dynamic behavior of the inverter circuit. (e) Hybrid complementary logic NOR, NAND gates and SRAM. Reprinted with permission from ref. 145. Copyright: 2009 WILEY-VCH.
7. Conclusions and outlook

In summary, the metal oxide nanowire family is a versatile group of materials with excellent electrical and optical properties and functions, which are promising building blocks for high performance and multifunctional TFTs. Various metal oxide nanowires like ZnO, In2O3 and SnO2 have been extensively explored to develop TFTs. Combining the operation rule of NW-FETs and the unique properties of metal oxide nanowires, the characteristics and performances of these transistors are flexible to be tuned and optimized effectively. The application of metal oxide NW-FETs spreads across an expansive area covering from transparent flexible electronics, different kind of sensing devices, to electronic memories and even integrated logic circuits. Until now, the intensive research interest in metal oxide NW-FETs have boosted the development of this field and abundant achievements have been attained. Looking into the future, there are more works should be launched.

First, as the ultimate limitation of device performances, properties of materials need to be studied. It has been demonstrated that doping is an effective method to control and improve the electrical properties. So the combinations of different dopants and host lattices need to be systematically explored, and new phenomena and properties may be found. On the other hand, ternary metal oxide nanowires are still an undeveloped area with many unknown characteristics remaining under cover, which should and will be studied in the future. As the processes related to the surface states play an important role in gas sensing, photodetecting, biosensing and carrier transport performances, systematic studies on reproducibly controlling the surface states will make a great contribution to the development of metal oxide NW-FETs. While n-type metal oxide nanowires have been intensively studied and presented great potential, p-type oxides or valid p-type doping strategies with comparable performances are still undiscovered. This is an important issue which must be settled in the future for CMOS circuit applications.

Another critical issue is optimizing the configuration and fabrication process of devices while taking the advantages of 1-dimensional geometric features of metal oxide nanowires. Metal contacting, structure of gating electrode and novel gating insulators will all be optimized. New fabrication process like self-templated methods will be also adopted to efficiently produce devices with minimized sizes and promoted performances.

At the same time, the applications of metal oxide NW-FETs will be developed in both longitudinal and crosswise ways. Sensing devices will have enhanced sensitivity and selectivity. Some smart sensing systems like “electronic noses” with high stability will complete the transition from “proof of concept” to practical application, by combining different metal oxide NW-FETs. The applications mentioned above can also be combined to form multifunction devices, such as transparent, flexible, and conformal sensors. Different technologies are considered to be integrated into a variety of systems with entire functions. For example, sensors can be equipped with self-powered elements and microwave communication components to serve as remote sensing networks.

Among various applications, transparent and flexible electronics based on metal oxide NW-FETs are probably the first field to be realized in industrial production, owing to the rapid development of consumer electronics and the urgent demand of novel display technology. Although some demonstrations of transparent and flexible AMOLED displays based on In2O3 nanowires have been carried out, the assembly of nanowires, stability and reproducibility of device performances are still the main obstacles before reaching such goal. More and more works will be concentrated in this exciting area and the problems will be solved based on the technics accumulated in the research directions mentioned above.

The breakthrough in these issues will facilitate the development of applications for memories and logic circuits, as well. Regarding the unique geometry of metal oxide nanowires, different designs of memories and logic circuits may come out. Once p-type metal oxide nanowires are prepared, and the mobilities of metal oxide nanowires are further improved comparable to bulk silicon, CMOS circuits based on metal oxide NW-FETs will be more attractive to the researchers. When the memories and logic circuits are combined with the features of transparency, flexibility and thin film energy storage technology, it is exciting to predict that computing on thin films will come true. Maybe, cellphones made of glasses or plastics are waiting for us!

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Notes and references
